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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,956	09/25/2003	Dean A. Klein	501303.01	9435

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EXAMINER	
PAN, JOSEPH T	
ART UNIT	**PAPER NUMBER**
2135	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,956	KLEIN ET AL.	
	Examiner	Art Unit	
	Joseph Pan	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-14, 16-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawaguchi (U.S. Pub. No. 2004/0088554 A1).

Referring to claim 1:

Kawaguchi teaches:

A processor-based electronic device, comprising:

a central processing unit ("CPU") (see figure 1, element 120a 'CPU' of Kawaguchi);

a system memory device coupled to the CPU (see e.g. figure 1, elements 104, 105 (RAM) of Kawaguchi);

a decryption engine coupled to the CPU, the decryption engine being operable to perform a decrypting function (see page 4, paragraphs [0059] – [0060] of Kawaguchi);

an integrated circuit package housing the CPU, the system memory device and the decryption engine so that interconnections between the CPU, the system memory device and the decryption engine are inaccessible from outside the

package (see figure 1, element 101 'a semiconductor integrated circuit device'; and page 4, paragraph [0049] of Kawaguchi); and

a source of a program in encrypted form, the source being external to the integrated circuit package and being coupled to the decryption engine, the encrypted program being decrypted by the decryption engine to allow the CPU to execute the program in unencrypted form (see figure 1, element D128a 'program'; and page 6, paragraph [0080] of Kawaguchi).

Referring to claims 2, 14, 26, 31-32, 34-35:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses a common semiconductor substrate (see figure 1, element 101 'a semiconductor integrated circuit device' of Kawaguchi).

Referring to claims 4, 16:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses a software decryption engine (see page 4, paragraphs [0059] – [0060] of Kawaguchi).

Referring to claim 5:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses the key storage device (see figure 1, elements 106-107 of Kawaguchi), and the decryption program storage device (see figure 1, element D123a 'decryption program' of Kawaguchi).

Referring to claims 6, 18, 28:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses the random access memory (see figure 1, elements 104-105 of Kawaguchi).

Referring to claims 7, 19, 27:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses the system controller (see figure 1, element 111a 'security controller' of Kawaguchi).

Referring to claims 8, 17, 20:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses that the decryption engine comprises a key storage device and a decryption engine unit (see figure 1, elements 106-107; and page 4, paragraphs [0059] – [0060] of Kawaguchi).

Referring to claims 9-11, 24, 29:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses the non-volatile memory (see figure 1, element D123a; and page 4, paragraph [0059], line 8 of Kawaguchi).

Referring to claim 12:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi further discloses the mass storage device (see figure 1, element 126 'pc' of Kawaguchi).

Referring to claim 13:

Kawaguchi teaches:

A secure processor module, comprising:

a central processing unit ("CPU") (see figure 1, element 120a 'CPU' of Kawaguchi);

a system memory device coupled to the CPU (see e.g. figure 1, elements 104, 105 (RAM) of Kawaguchi);

a decryption engine coupled to the CPU, the decryption engine being operable to perform a decrypting function (see page 4, paragraphs [0059] – [0060] of Kawaguchi); and

an integrated circuit package housing the CPU, the system memory device and the decryption engine so that interconnections between the CPU, the system memory device and the decryption engine are inaccessible from outside the package (see figure 1, element 101 'a semiconductor integrated circuit device'; and page 4, paragraph [0049] of Kawaguchi).

Referring to claims 21-22:

Kawaguchi discloses the claimed subject matter: a secure processor module (see claim 13 above). Kawaguchi further discloses the data path (see e.g. figure 1, the data link between element 120a 'cpu' and element 104 'RAM', of Kawaguch).

Referring to claim 23:

Kawaguchi teaches:

A processor-based electronic device, comprising:

an integrated circuit package (see figure 1, element 101 'a semiconductor integrated circuit device'; and page 4, paragraph [0049] of Kawaguchi);

a CPU housed within the integrated circuit package (see figure 1, element 120a 'CPU' of Kawaguchi);

a system memory device housed within the integrated circuit package (see e.g. figure 1, elements 104, 105 (RAM) of Kawaguchi);

an external interface circuit housed within the integrated circuit package (see figure 1, element 111a 'security controller' of Kawaguchi);

a first plurality of conductors coupling the CPU to the system memory device and to the external interface circuit, the first plurality of conductors being housed within the integrated circuit package and being inaccessible from outside the integrated circuit package (see page 5, paragraph [0066] of Kawaguchi);

a second plurality of conductors coupled to the external interface circuit, at least some of the second plurality of conductors extending outside the integrated circuit package so that the conductors are accessible from outside the integrated circuit package (see page 5, paragraph [0066] of Kawaguchi); and

a source of a program in encrypted form, the source being external to the integrated circuit package and being coupled to at least some of the second plurality of conductors that extend outside the integrated circuit package (see figure 1, element D128a 'program'; and page 6, paragraph [0080] of Kawaguchi).

Referring to claim 25:

Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 23 above). Kawaguchi further discloses the program (see figure 1, element d128a 'program' of Kawaguchi).

Referring to claim 30:

Kawaguchi teaches:

A method of securely executing a computer program in a processor-based electronic device having a central processing unit ("CPU");, a system memory, and an external interface circuit, the method comprising:

encrypting a computer program that is to be executed by the CPU (see figure 1, element D128a 'program'; and page 4, paragraph [0061], lines 5-6 of Kawaguchi);

coupling the computer program to the external interface device (see page 4, paragraphs [0059] – [0060] of Kawaguchi);

decrypting the computer program after the computer program has been coupled to the external interface device, the computer program being shielded from access after being decrypted (see page 4, paragraphs [0059] – [0060] of Kawaguchi);

executing the decrypted computer program using the CPU (see page 5, paragraph [0070], lines 10-12 of Kawaguchi); and

during the execution of the computer program, coupling data between the CPU and the system memory, the data being shielded from access while being coupled between the CPU and the system memory (see abstract, lines 1-4 'When an encrypted program and a decryption program are inputted to a first memory, a semiconductor integrated circuit device causes a bus port to disable access from the outside,', of Kawaguchi, emphasis added).

Referring to claim 33:

Kawaguchi discloses the claimed subject matter: a method of securely executing a computer program in a processor-based electronic device (see claim 30 above). Kawaguchi further discloses storing a decryption key in a key storage device; coupling the decryption key from the key storage device to a decryption engine; coupling the computer program from the external interface device to the decryption

engine; using the decryption engine to decrypt the computer program based on the decryption key. (see page 4, paragraphs [0059] – [0060] of Kawaguchi).

Referring to claims 36, 38:

Kawaguchi discloses the claimed subject matter: a method of securely executing a computer program in a processor-based electronic device (see claim 30 above). Kawaguchi further discloses using the CPU to execute the computer program stored in the system memory (see page 4, paragraphs [0059] – [0060] of Kawaguchi).

Referring to claim 37:

Kawaguchi discloses the claimed subject matter: a method of securely executing a computer program in a processor-based electronic device (see claim 30 above). Kawaguchi further discloses using the transferring (see page 4, paragraphs [0059] – [0060] of Kawaguchi).

Referring to claim 39:

Kawaguchi discloses the claimed subject matter: a method of securely executing a computer program in a processor-based electronic device (see claim 30 above). Kawaguchi further discloses coupling the computer program from the program storage device to the external interface device (see figure 1, element 126 'pc', element 110a 'bus port' of Kawaguchi).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi (U.S. Pub. No. 2004/0088554 A1) in view of Deng et al. (U.S. Patent No. 6,701,432 B1).

Referring to claims 3, 15:

i. Kawaguchi discloses the claimed subject matter: a processor-based electronic device (see claim 1 above). Kawaguchi discloses a software decryption engine (see page 4, paragraphs [0059] – [0060] of Kawaguchi). However, Kawaguchi does not specially mention to a hardware decryption engine.

ii. Deng teaches a gateway for screening packets transferred over a network, wherein Deng discloses a hardware decryption engine (see figure 4, element 402 'encryption/decryption(DBS, Triple-DBS) engine' of Deng).

iii. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Deng into the method of Kawaguchi to use a hardware decryption engine.

iv. The ordinary skilled person would have been motivated to have applied the teaching of Deng into the system of Kawaguchi to use a hardware decryption engine, because "The solution is implemented in hardware, easily handling dense traffic that would have choked a conventional firewall. A combination firewall and VPN (virtual private network) solution is provided that includes a separate stand-alone firewall engine, encryption/decryption engine and authentication engine. Each engine operates independently and exchanges data with the others. One engine can start processing data without waiting for other engines to finish all their processes. Parallel processing and pipelining are provided and deeply implemented into each engine and each module further enhancing the whole hardware solution. The high processing speed of hardware increases the throughput rate by a factor of ten." (see column 4, lines 10-17 of Deng).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Pan whose telephone number is 571-272-5987.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached at 571-272-3859. The fax and phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Joseph Pan
February 1, 2007

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100